A B S T R A C T

A channel estimation circuit (12) of an individual CH path demodulation unit (1A - 1L) performs a channel estimation from an individual CH. A channel estimation value correction circuit (22) of a shared CH path demodulation unit (2A - 2L) then corrects a reception power fluctuation due to uplink transmission power control which is caused by the timing offset between the individual CH and the shared CH. The resultant data is used for the demodulation by a shared CH demodulation circuit (23).